REMARKS/ARGUMENTS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this Application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-21 in the application. The Applicants have amended independent Claims 1, 8, 12 and 15 and have canceled dependent Claims 5 and 19. The Applicants have added dependent Claims 22 and 23. Accordingly, Claims 1-4, 6-18 and 20-23 are currently pending in the Application.

I. Rejection of Claims 1-21 under 35 U.S.C. §102

The Examiner has rejected Claims 1-21 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,221,774 to Henry et al. ("Henry"). As the Examiner is no doubt aware, anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference; the disclosed elements must either be disclosed expressly or inherently and must be arranged as in the rejected claims.

As discussed in the previous amendment, Henry relates to the prediction of conditional branch instruction outcomes associated with a microprocessor having a pipeline architecture. (*See* column 1, lines 8-10.) Henry discloses a microprocessor 100 having a fetcher 101 that fetches instructions according to the contents of an instruction pointer (IP) 142. The microprocessor 100 also includes a branch predictor 103 that controls the selection of the contents to be loaded into the IP 142 based upon a prediction of whether a conditional branch instruction will be taken. (*See* column 6, line 53 to column 7, line 16.) The branch instruction address is piped downed with the

branch instruction through the various stages of the microprocessor pipeline via registers. (*See* column 7, lines 28-31.) The branch predictor 103 also indicates information relating to its static prediction of the outcome of a conditional branch. The static prediction information is stored in a static prediction register and is piped down with the conditional branch instruction through the various stages of the pipeline via static predictor registers. (*See* column 7, lines 44-53.)

Amended independent Claim 1 is directed to a mechanism for identifying and tracking conditional instructions for use in a wide-issue processor. Amended independent Claim 1 recites a conditional execution block state machine that tags and generates *contemporaneous* link pointers for instructions located in a conditional execution block, *wherein the link pointers market least the beginning and end of a conditional execution block of instructions*. Amended independent Claim 1 further recites conditional link pointer register sets, wherein each of the sets corresponds to a stage of a pipeline of said processor that contain and cause the link pointers to move through each of the sets as said instructions associated with the link pointers and located in the conditional execution block move through each of the corresponding stages. In the present Application, "contemporaneous" may be generally defined as "originating at substantially the same period of time."

The Office Action states, regarding former dependent claim 5, which has been used as a basis for the above amendment of claim 1:

> Referring to claim 5, Henry has taught ... where said execution block state machine generates said link pointers that mark the beginning and end of a conditional execution block of instructions (Column 10, lines 11-23, Instruction pointers that point to a taken branch target address mark the beginning of a conditional execution block of instructions. On a branch taken misprediction, the instruction pointer marks the end of the conditional execution block of instructions by pointing to the next sequential instruction.) (Office Action, page 4.)

Applicants respectfully disagree with the characterization of Henry made by the Office Action as applied to the claim language of Claim 1. Column 10, lines 11-23 of Henry state:

> The Agree/Disagree bits are updated via update signal 456 generated by comparator 406. Comparator 406 receives static prediction 130 via signal 183 made by static predictor 222 and compares the static prediction 130 with the actual result, or outcome, 110 of the conditional branch instruction, received via signal 184. If static predictor 222 incorrectly predicts the outcome of the conditional branch instruction, then history table 402 is updated with a Disagree value as indexed by index generation logic 412. However, if static predictor 222 correctly predicts the outcome of the conditional branch instruction, then history table 402 is updated with an Agree value.

In Henry, there is no conditional execution block state machine that tags and generates *contemporaneous* link pointers for instructions located in a conditional execution block, *wherein the link pointers mark the beginning and end of a conditional execution block of instructions.* Instead, in the cited passage of Henry as applied to previous dependent claim 5, a history table 402 is updated with disagree or agree values, as appropriate. However, the asserted '... end of the conditional execution block of instructions' as referred to by the Office Action are determined *after* an actual result is compared to a predicted outcome of a conditional branch instruction. In claim 1 as amended, however the link pointers are *contemporaneous.*

In some embodiments, employment of contemporaneous link pointers allow for advantages not found in the cited prior art. For instance, the present Application states:

> The CE logic block *isu_cexe* 220 is responsible for identifying CE (*cexe*) instructions and *tagging the beginning and ending instructions of the cexe blocks that they define in the queue 211.* When instructions in a *cexe* block are provided to the GR stage, they are specially tagged to ensure that the instruction grouping logic 263 groups them for optimal execution. (Present Application, page 18, paragraph 41; emphasis added).

Therefore, Henry does not disclose each and every element of Claim 1 and as such, is not an anticipating reference, or its dependent claims. Henry also is not an anticipating reference for Claims 8 and 15, as they contain at least some language that is analogous to independent Claim 1. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection with respect to these Claims, and their dependent claims.

Henry does not anticipate new Claims 22 and 23, because they depend upon independent claims 1 and 8, respectively, which Applicants respectfully state are now also allowable.

II. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-4, 6-18 and 20-23. Applicants reserve the right to address future arguments that were not raised in the current amendment.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 12-2252.

Respectfully submitted,

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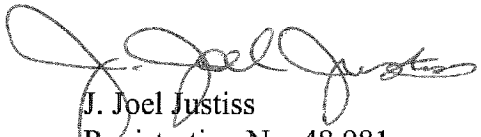

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